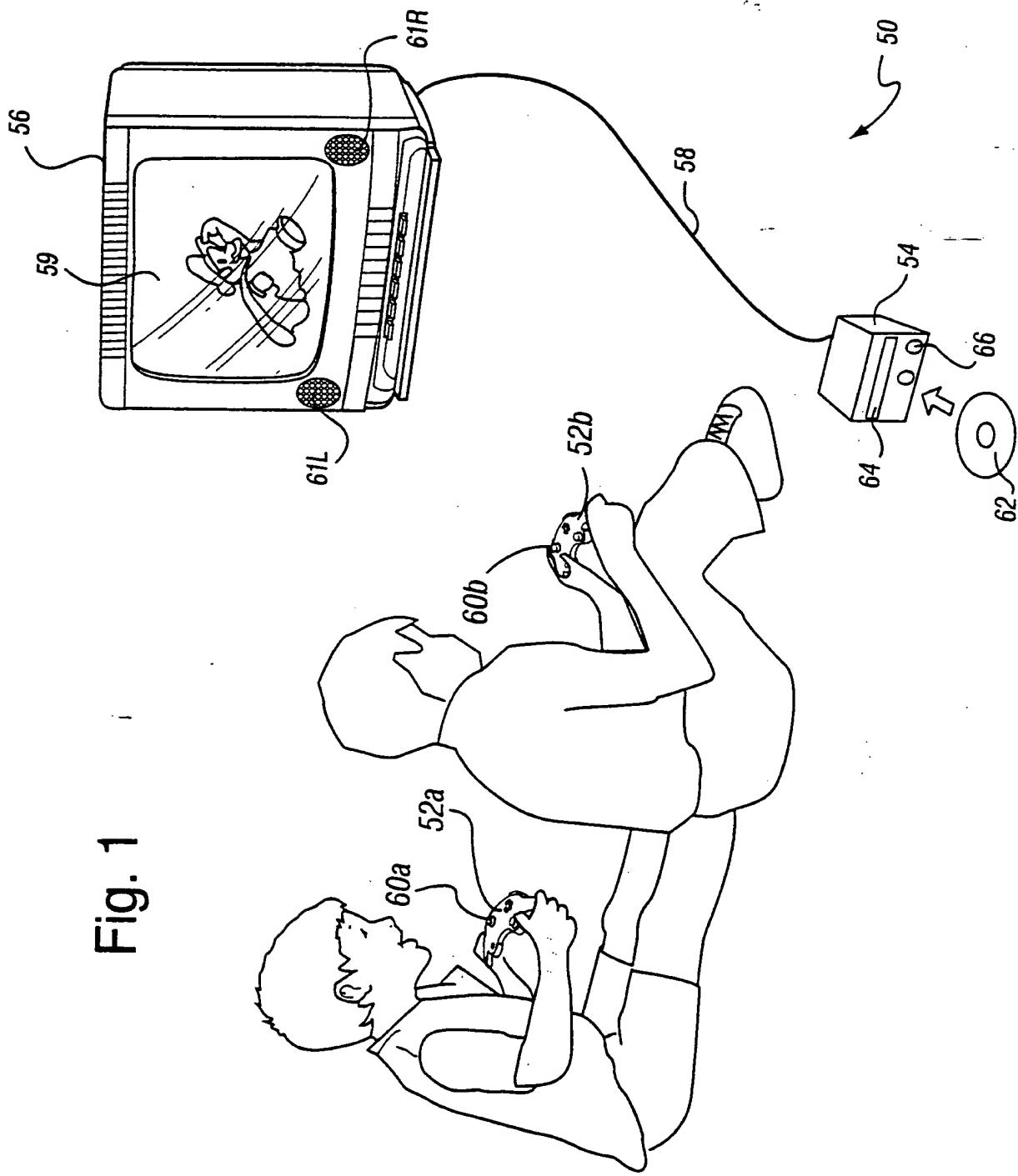


Fig. 1



1818

23

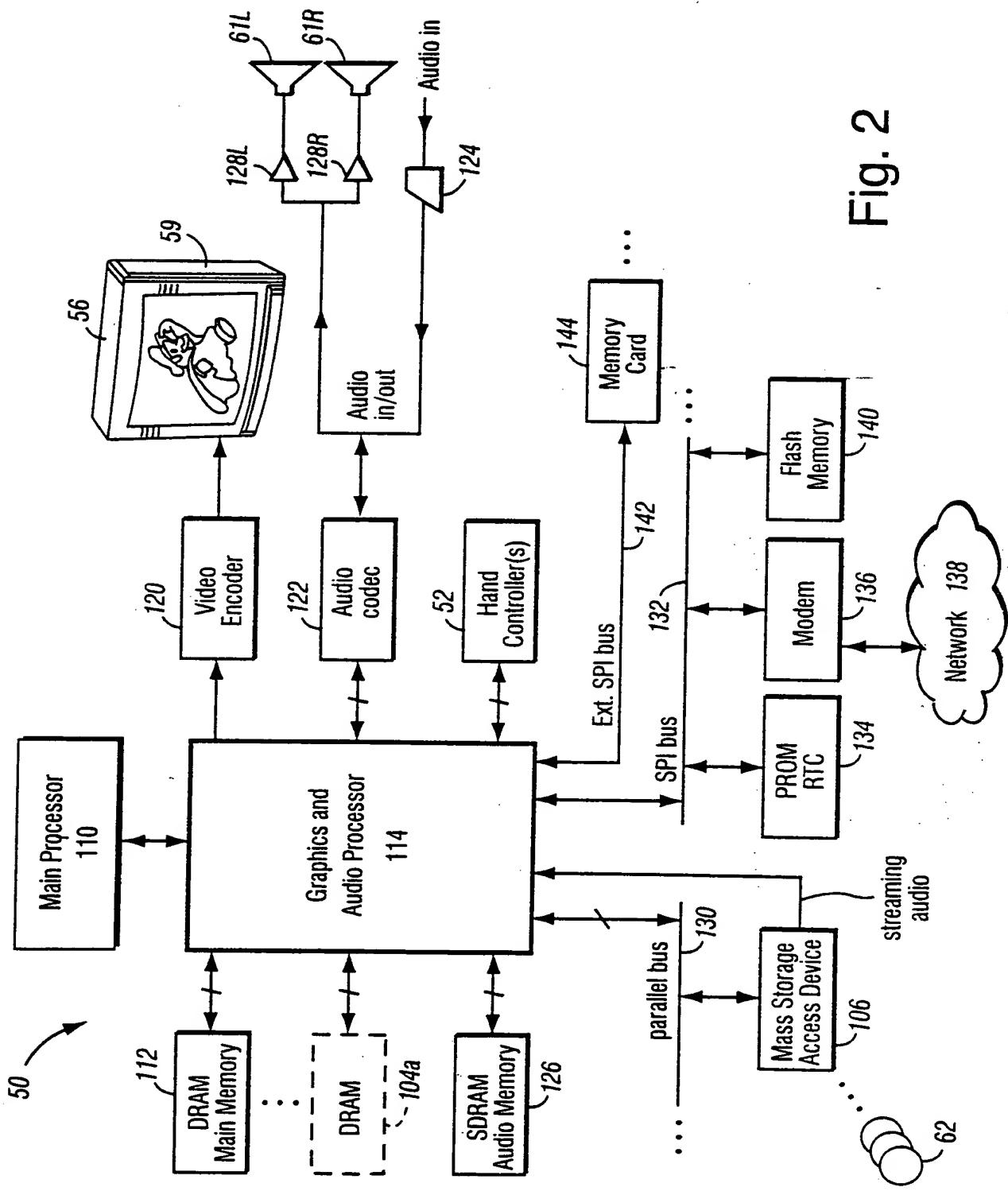


Fig. 2

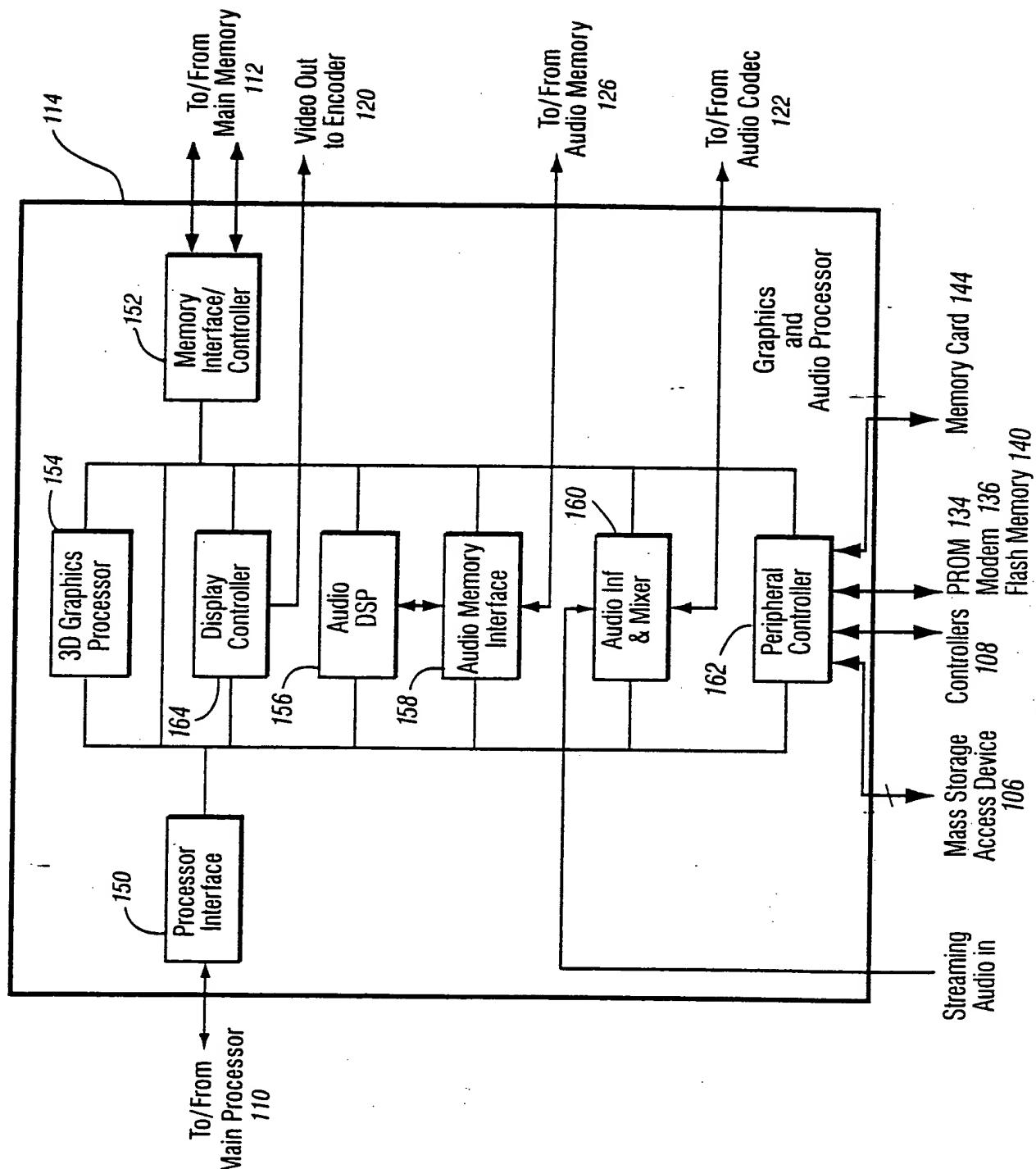


Fig. 3

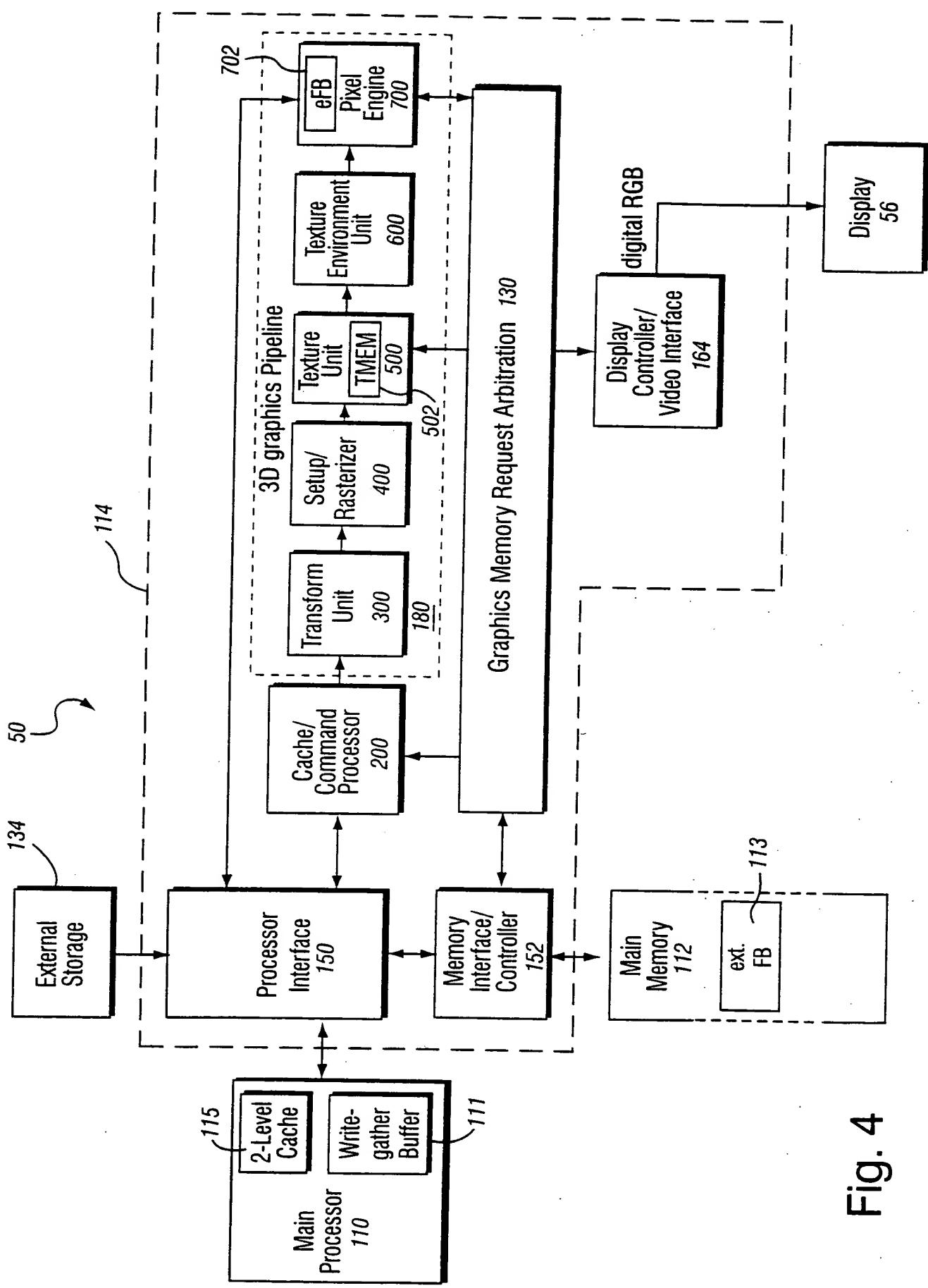


Fig. 4

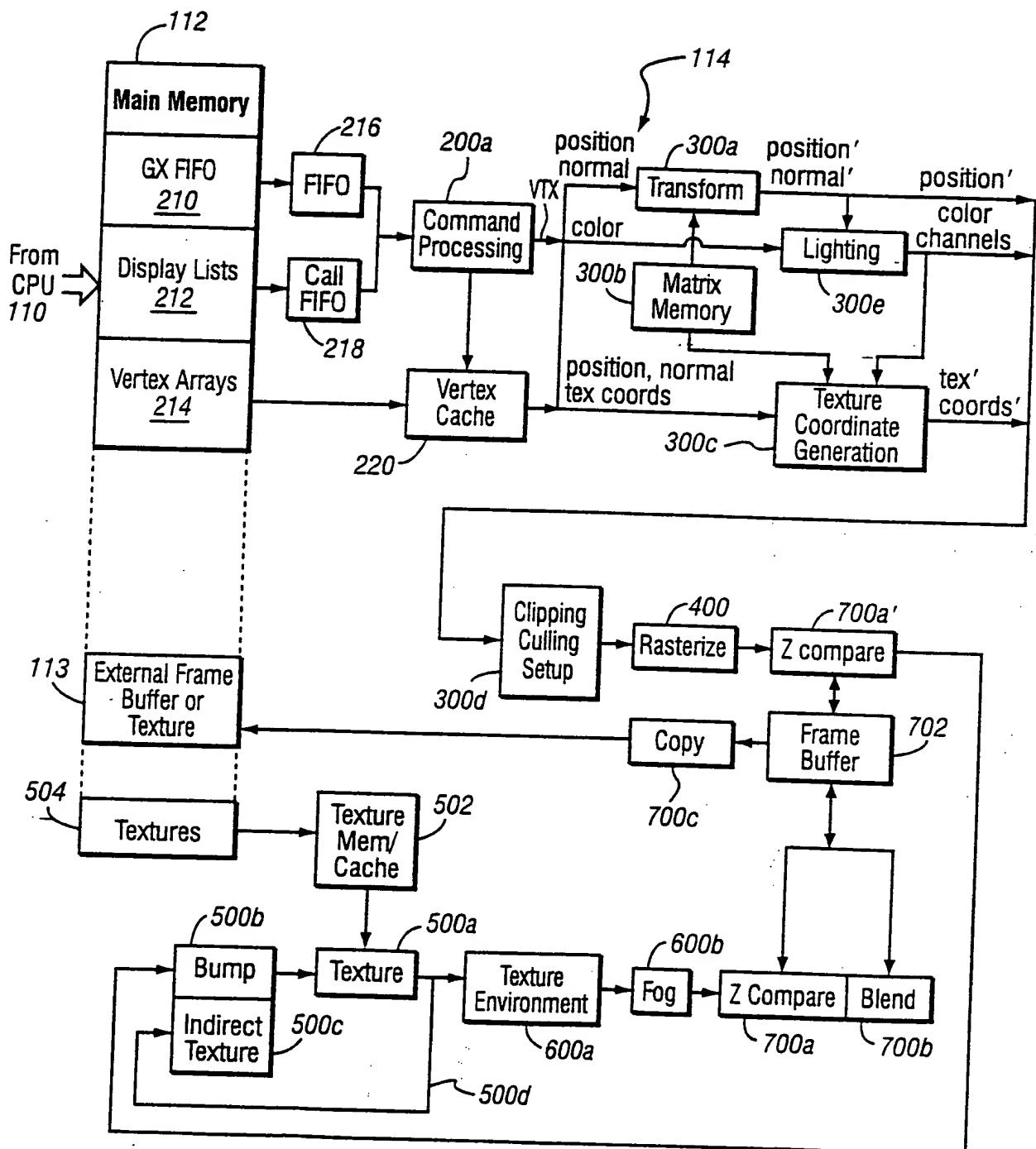
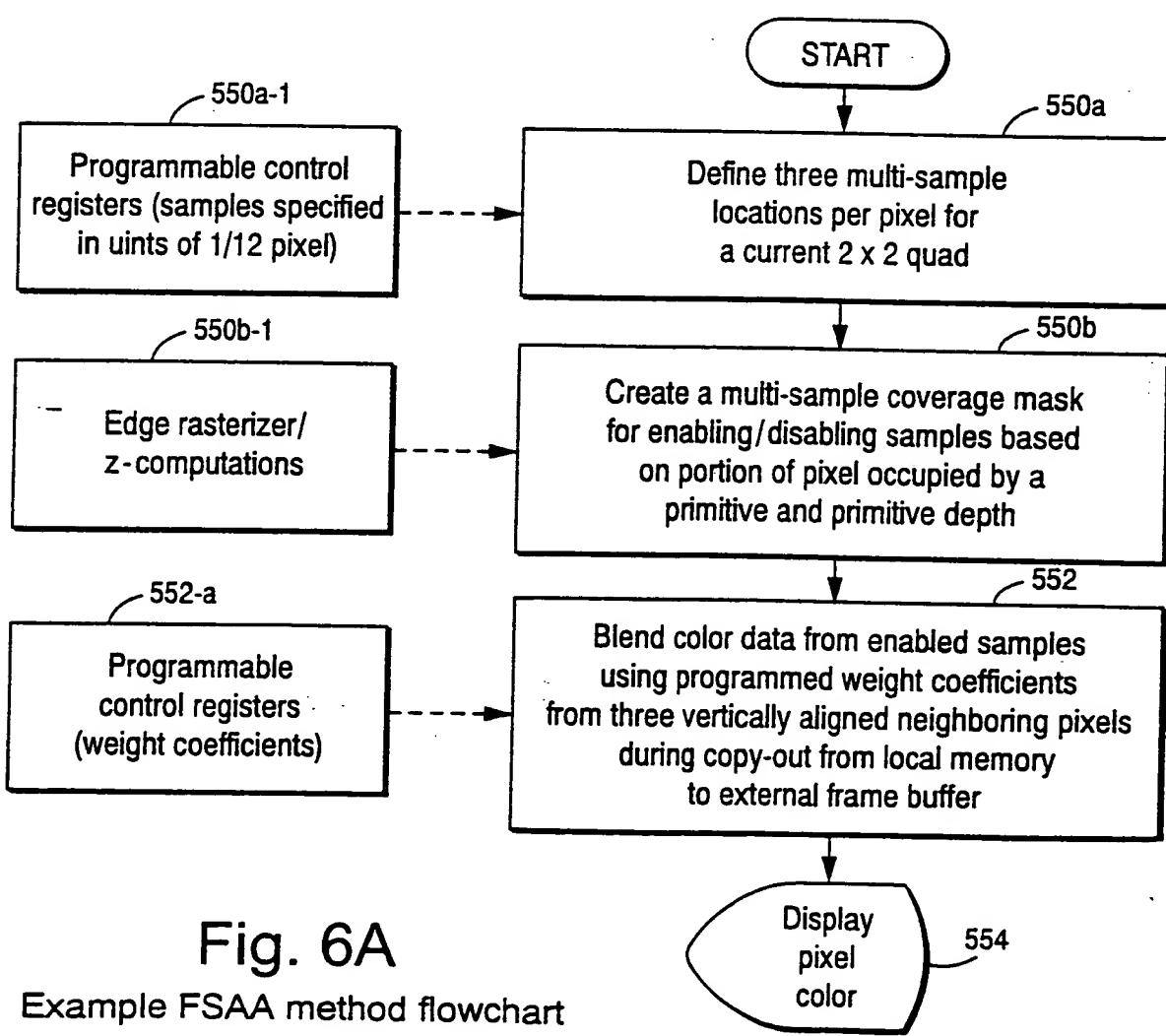
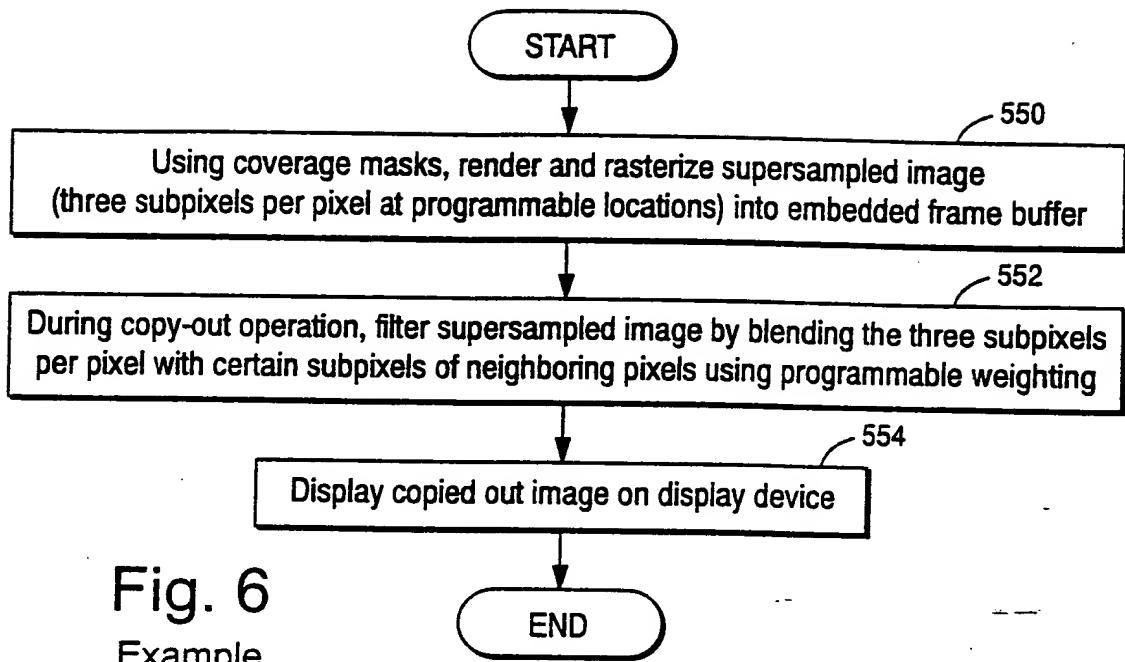


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

69/18



7/18

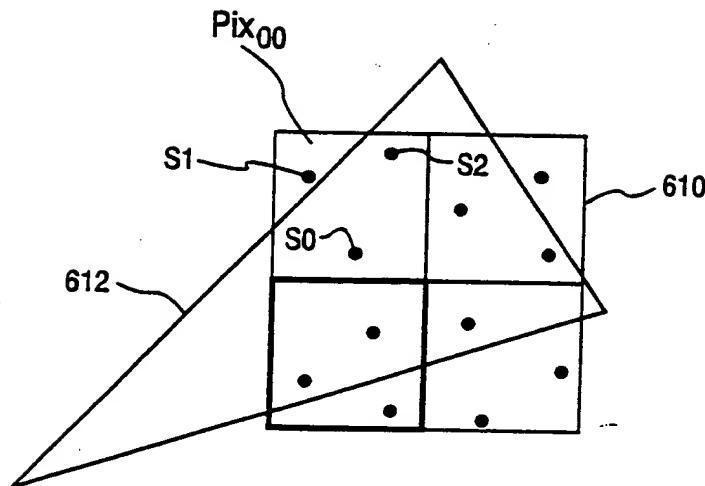


Fig. 7
(Primitive and super-sampled piexel quad)

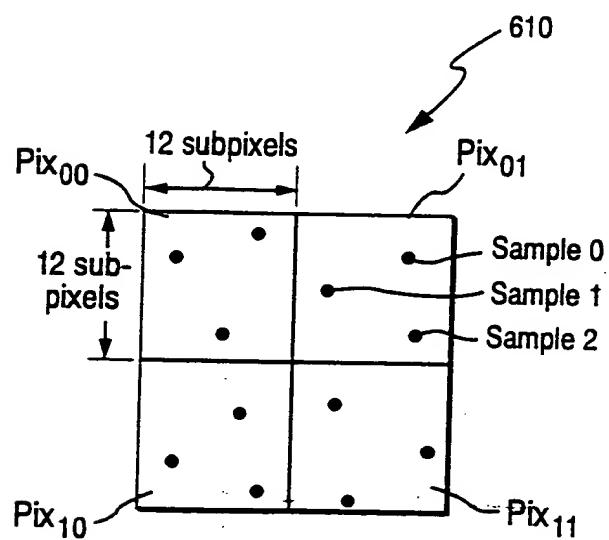


Fig. 8
(Sampling pattern)

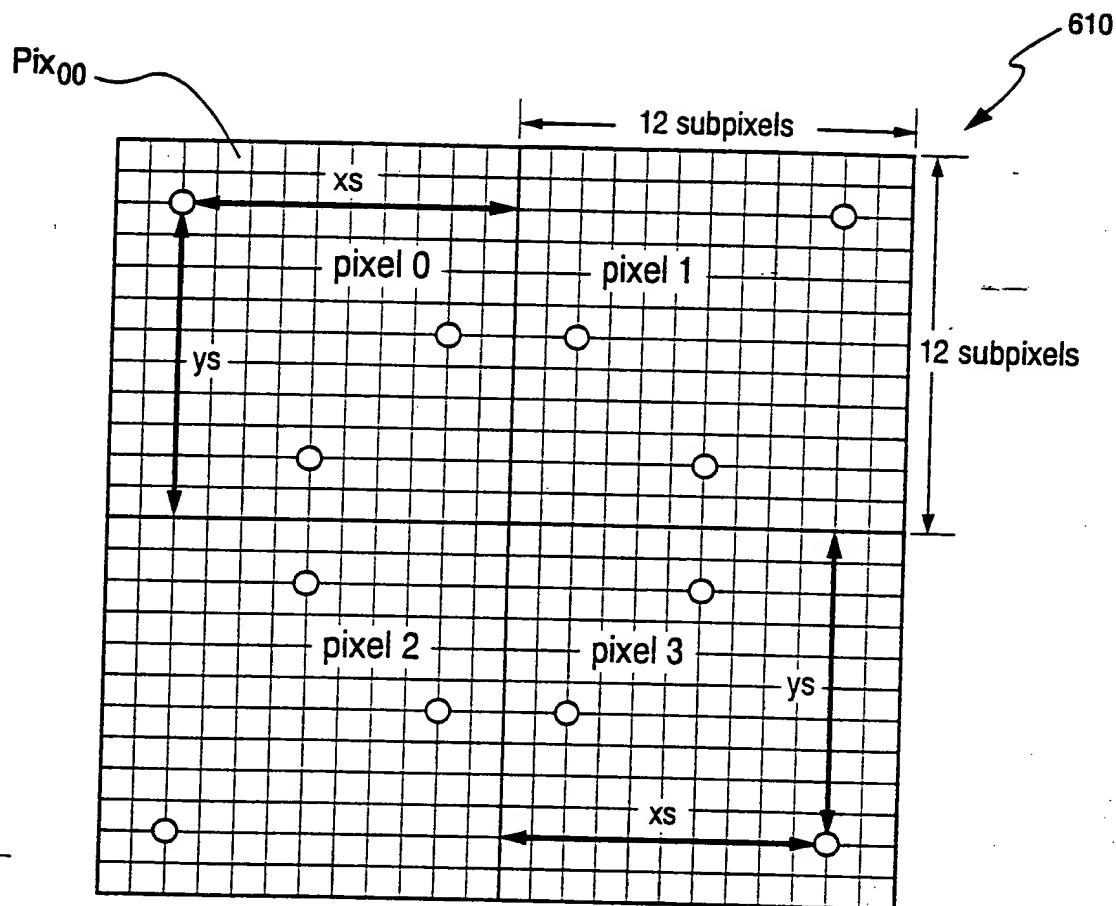


Fig. 9 (Super-sample locations in units of 1/12 pixel)

9/8/18

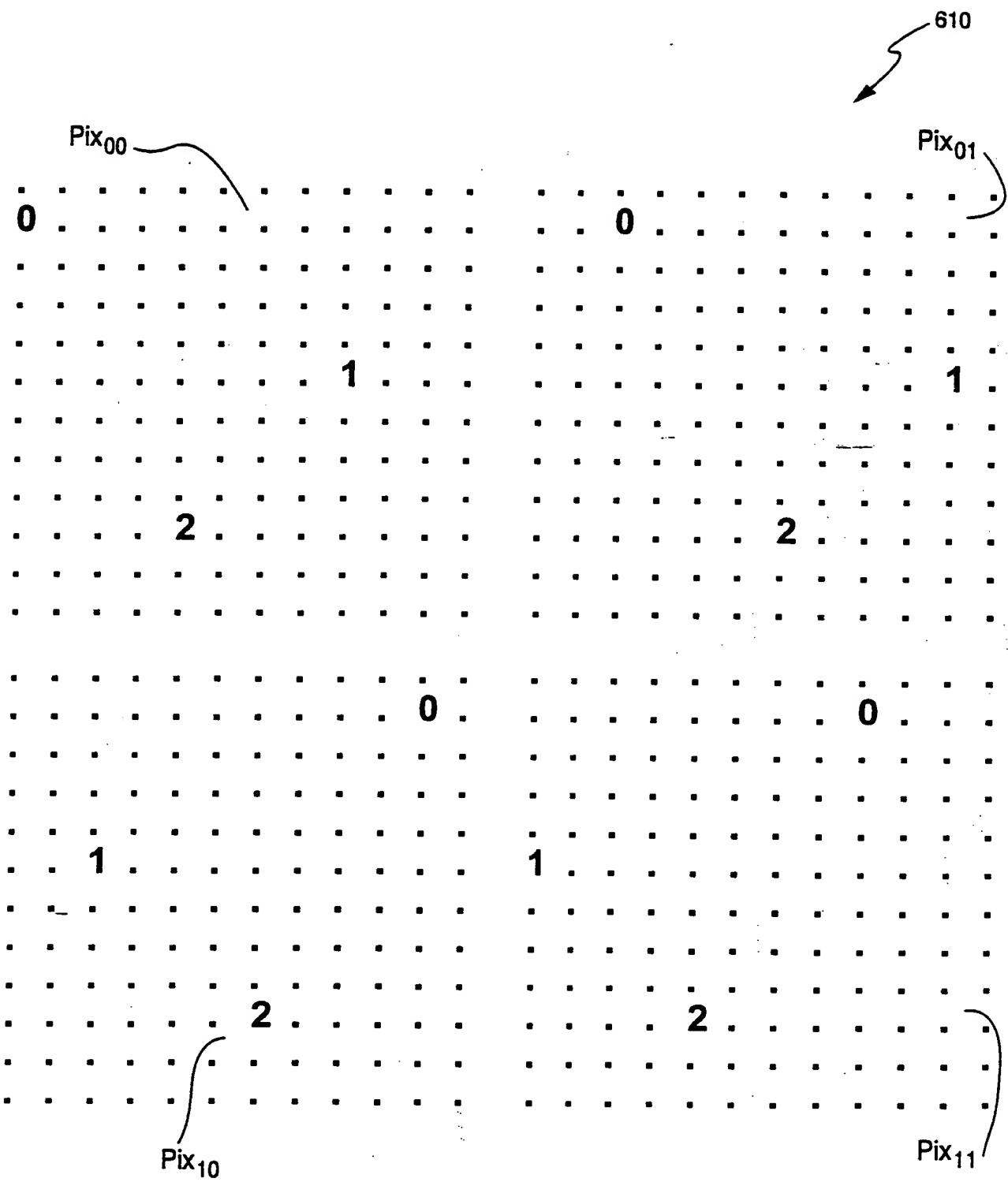


Fig. 10 (Preferred sampling pattern)

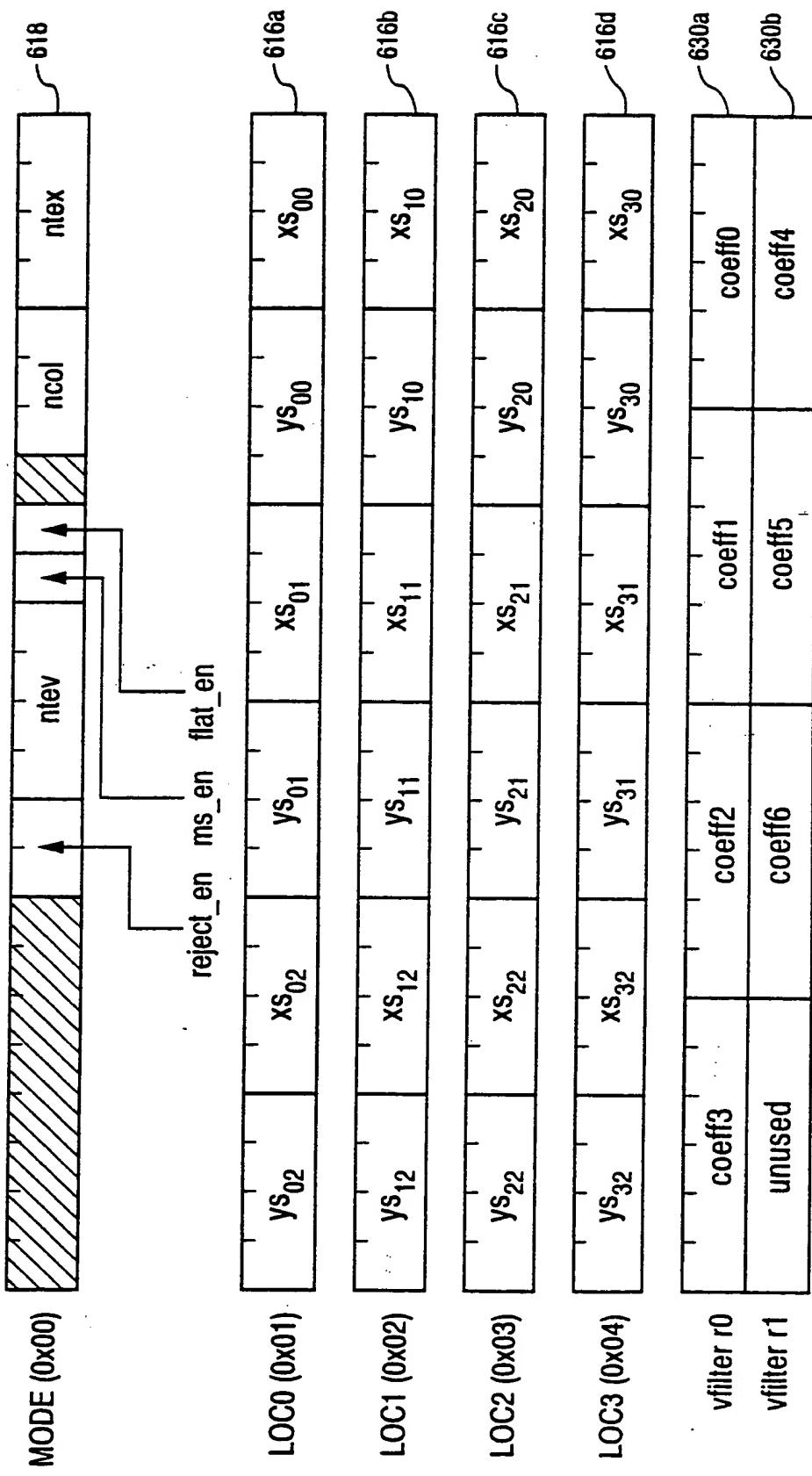
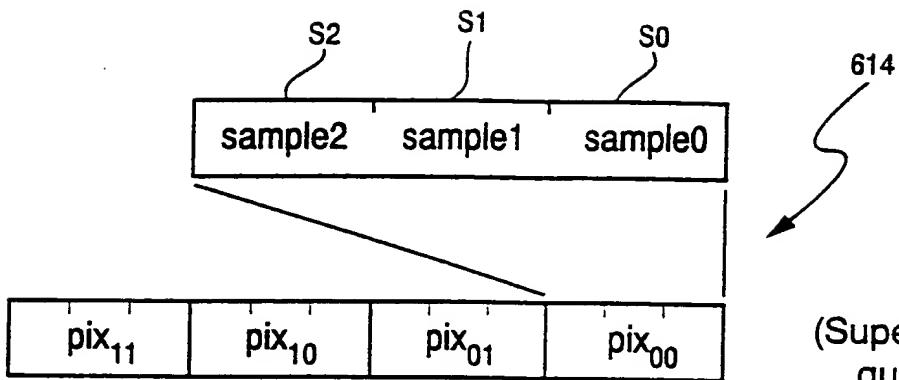


Fig. 11 (Programmable control registers for setting sample locations & filter coefficients)



11/8/18
Fig. 12
(Super-sampling for current quad-coverage mask)

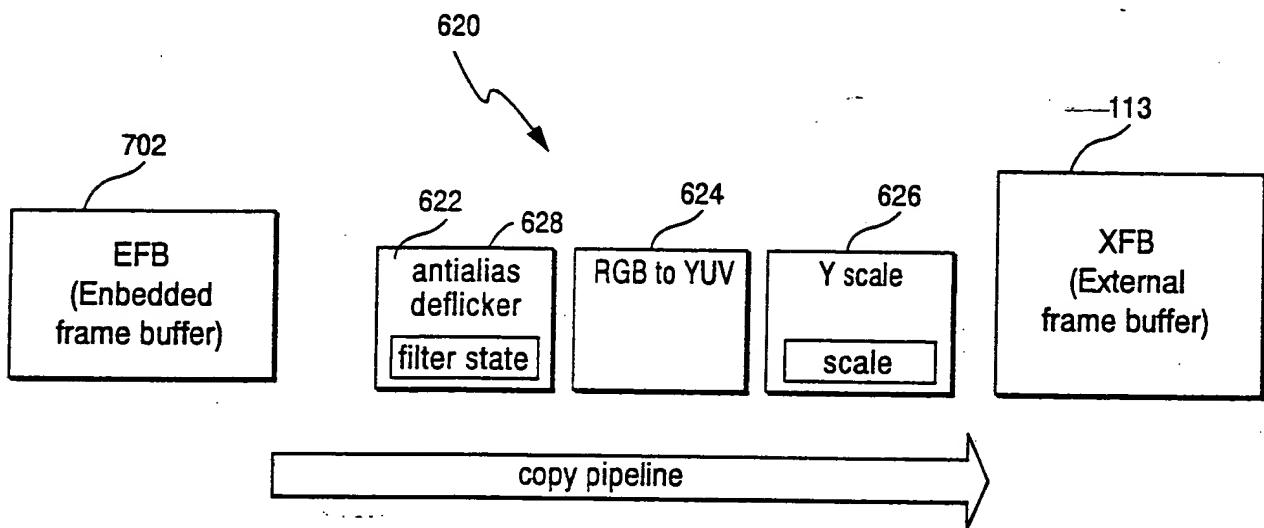


Fig. 13 (Copy-out pipeline)

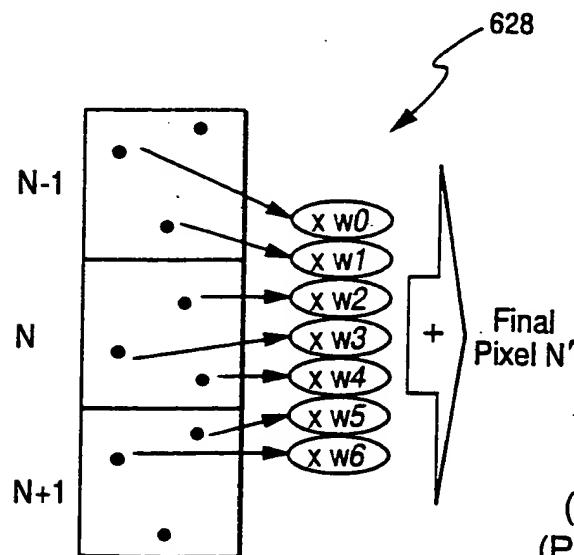


Fig. 14
(Vertical Filter Blending)
(Programmable 7-tap filter)

12/18

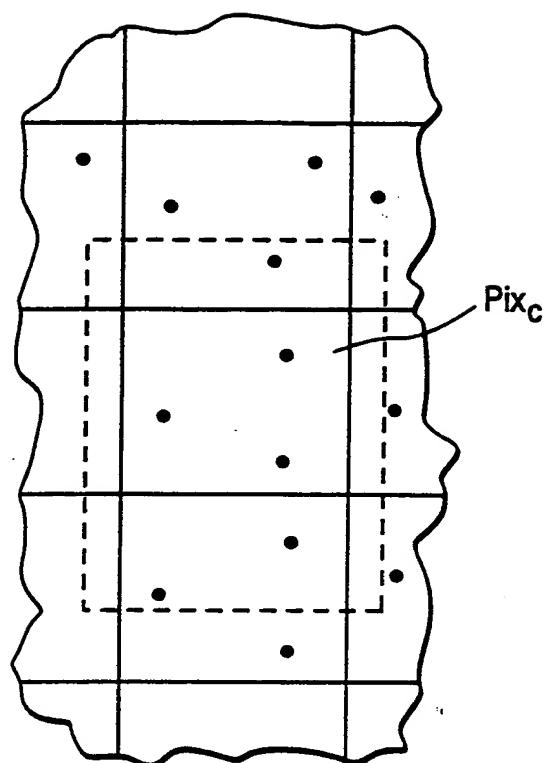


Fig. 15
Example vertical filter aperture

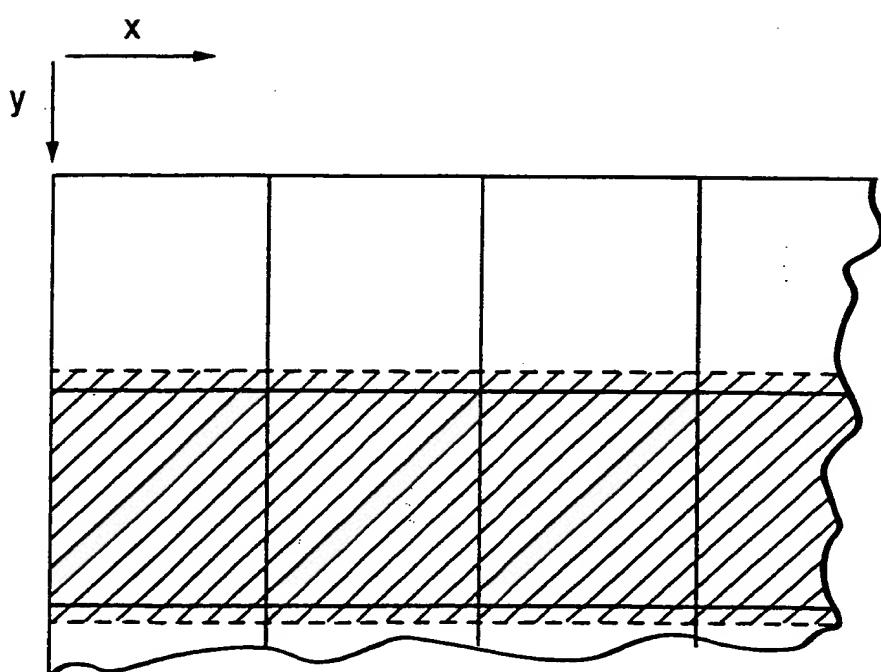
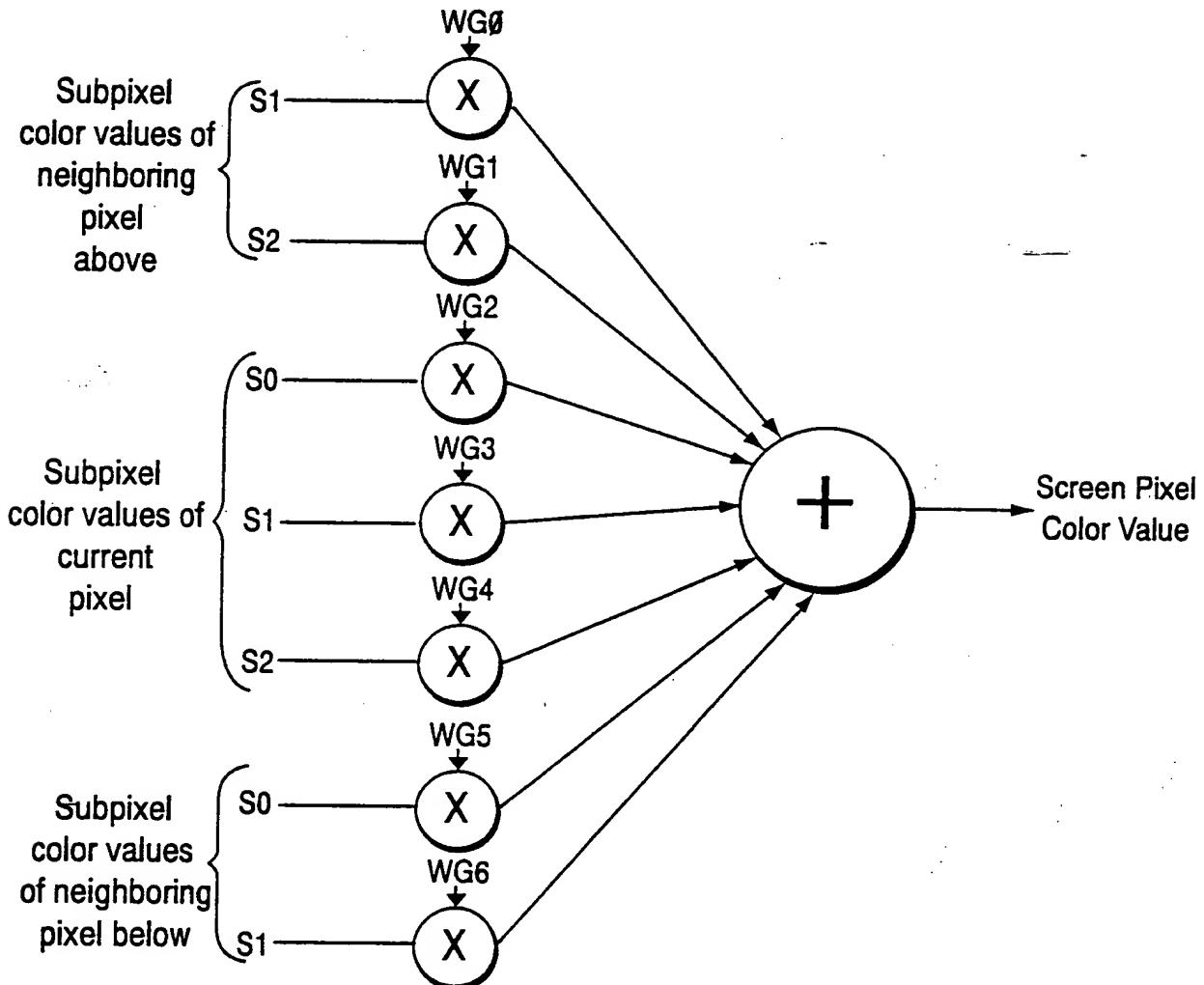


Fig. 17
Example AA copy out buffering

13/18
Fig. 16
(Example Vertical Filter Structure)



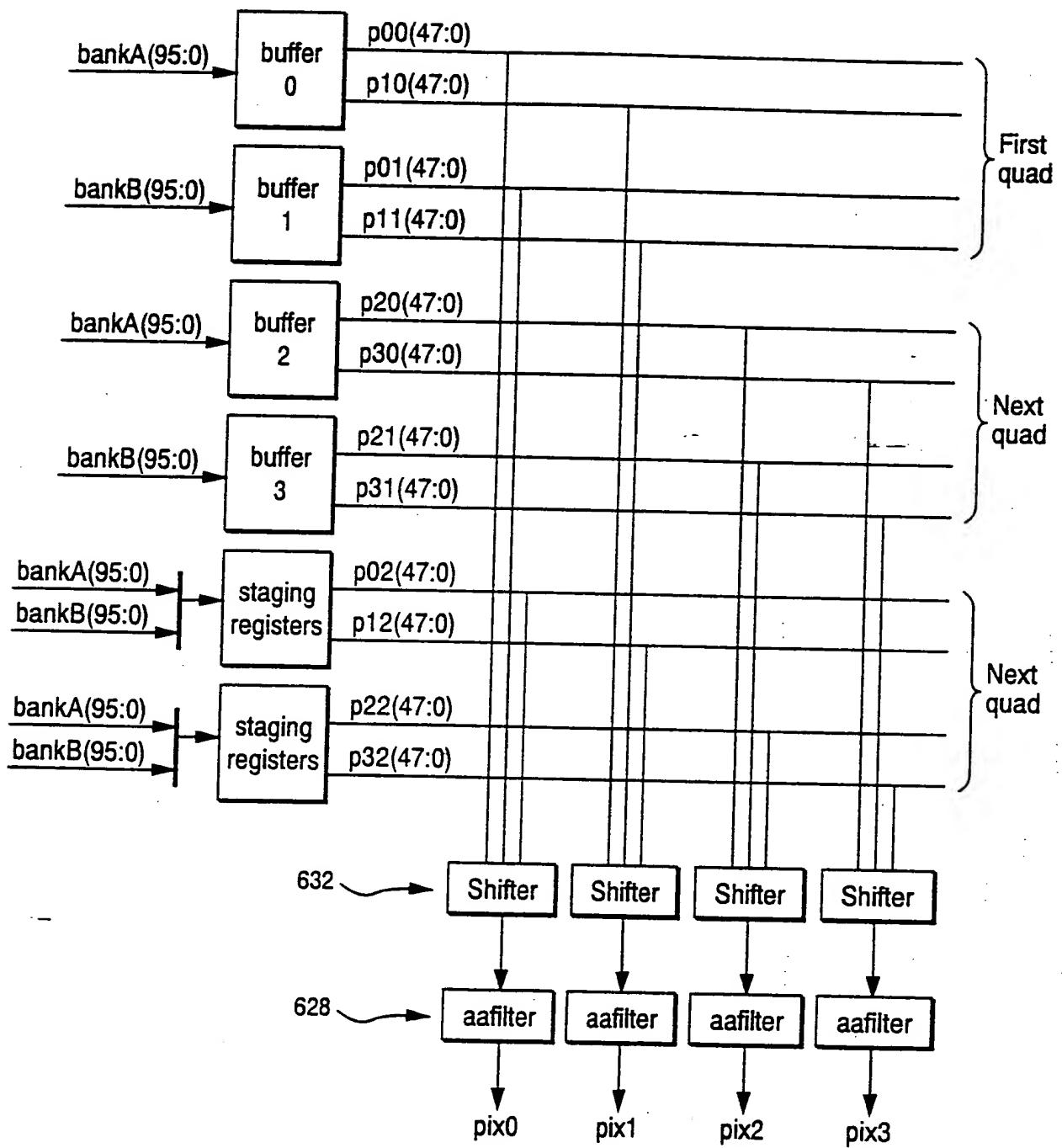


Fig. 18
(AA buffering)

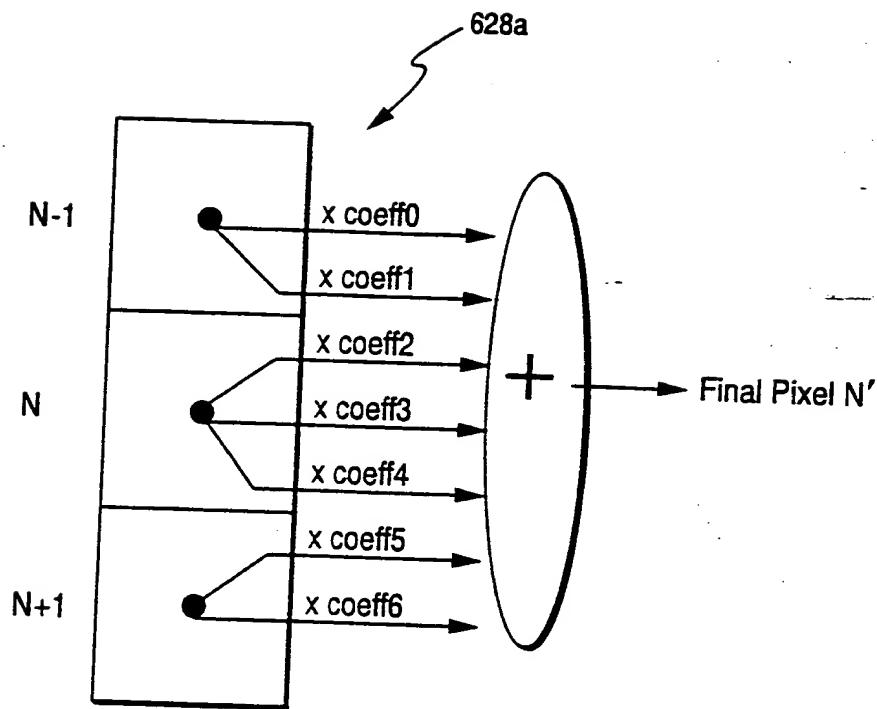


Fig. 19
Example de-flickering filter

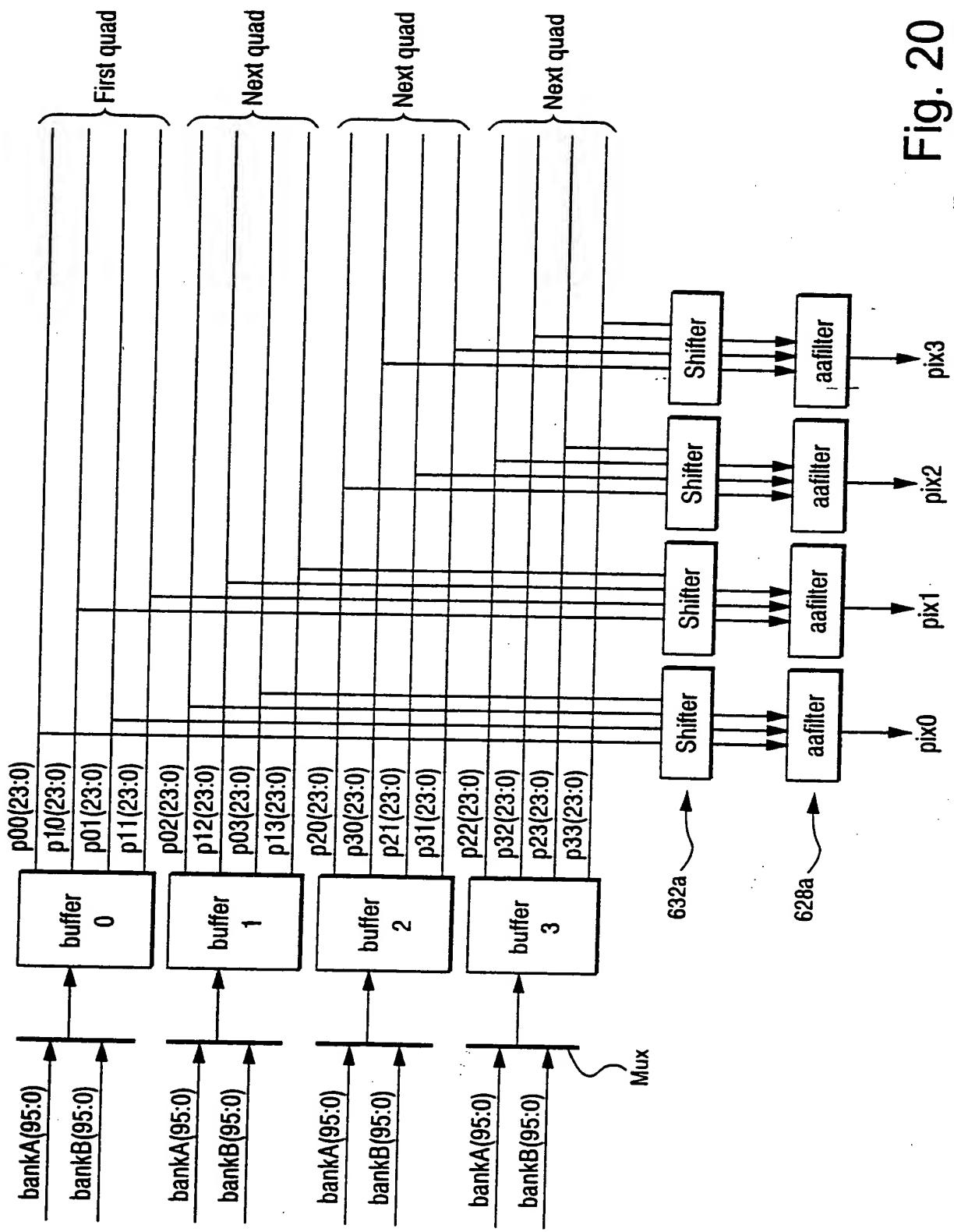


Fig. 20
(De-flicker buffering)

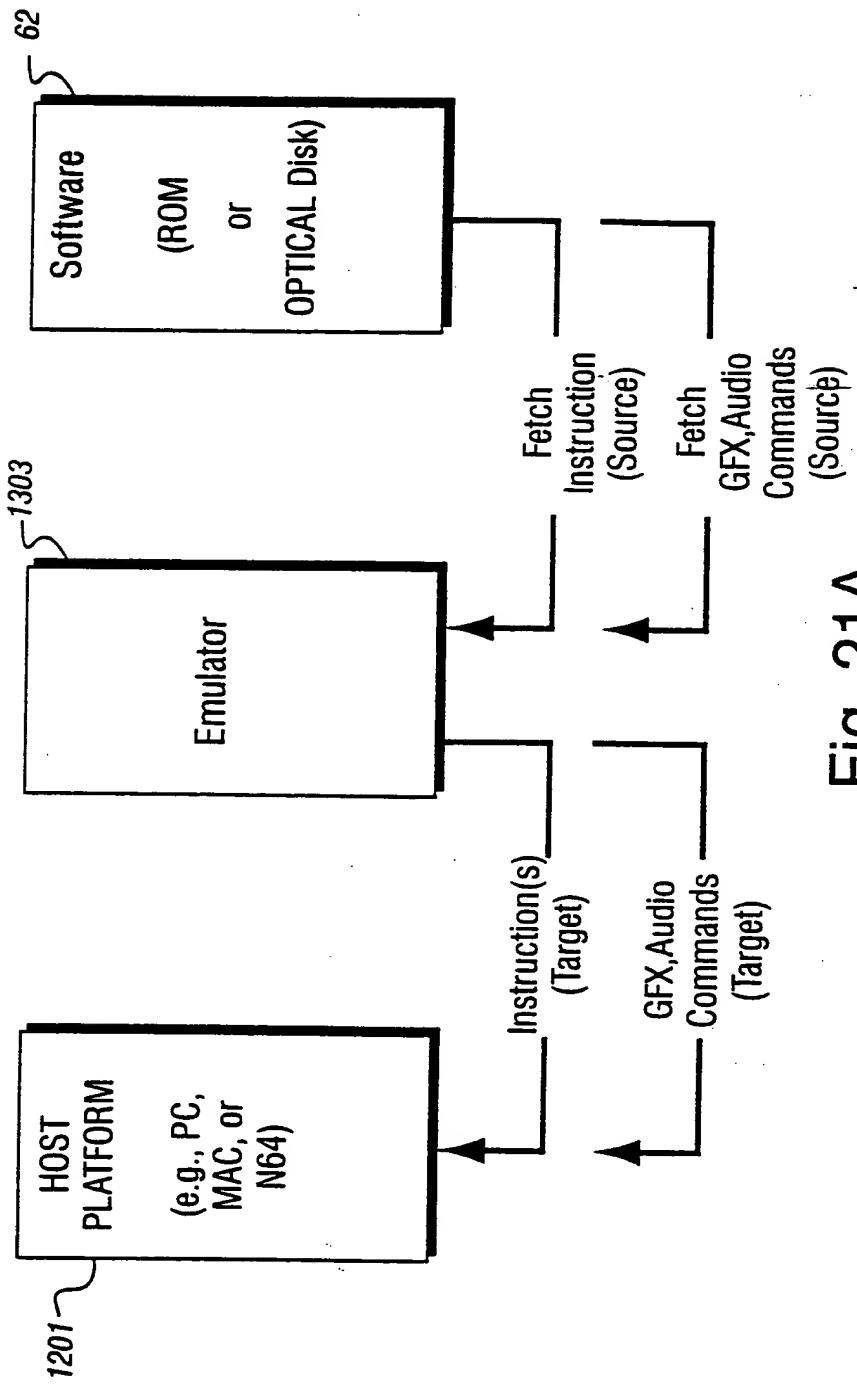


Fig. 21A

